

North South University

Center of Excellence in Higher Education

CSE231.2

Term Project-SP18

Phase 1: Combinational Circuit Design and Implementation

Group : **7**

Group Members:

|  |  |
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Submitted to:

**Dr. Arshad M. Chowdhury**

Submission date: 11.03.2018

**Objectives:**

* Design a complete logic system from specification to implementation
* Coordination between the combinational and the sequential parts
* Become familiarized with the analysis of combinational logic networks and Synchronous Sequential Logic
* Learn the implementation of networks using Logic gates, decoders or MUX
* We need to display “**SP18-CSE231-7**” if the Direction input is logic **LOW** and the reverse order (“**7-132ESC-81PS**”) if the Direction input is logic **HIGH**

**Phase 1: Combinational Circuit Design and Implementation**

**List of Equipment:**

* IC 74151 (8:1 Multiplexers)
* IC 7404 (NOT Gates)
* Seven-Segment Display
* Voltage Regulator
* Voltage source1
* Breadboard
* Switch
* Wires

**Part A (Using basic logic gates)**

**Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **A** | **B** | **C** | **D** | **Fa** | **Fb** | **Fc** | **Fd** | **Fe** | **Ff** | **Fg** |  |
| **0** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | **S** |
| **1** | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | **P** |
| **2** | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | **1** |
| **3** | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **8** |
| **4** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **-** |
| **5** | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | **C** |
| **6** | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | **S** |
| **7** | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | **E** |
| **8** | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | **2** |
| **9** | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | **3** |
| **10** | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | **1** |
| **11** | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **-** |
| **12** | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | **7** |
| **13** | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| **14** | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |
| **15** | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**Sum of Product (SOP):**

Fa (A,B,C) = (0,1,3,5,6,7,8,9,12)

Fb (A,B,C) = (1,2,3,8,9,10,12)

Fc (A,B,C) = (0,2,3,6,9,10,12)

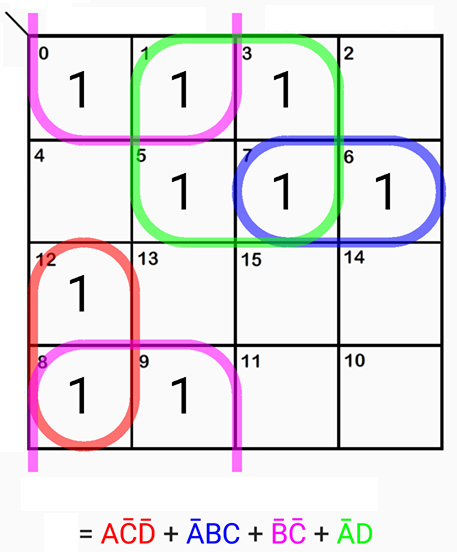
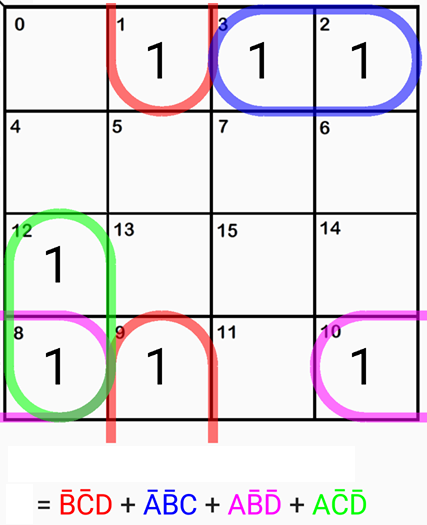
Fd (A,B,C) = (0,3,5,6,7,8,9)

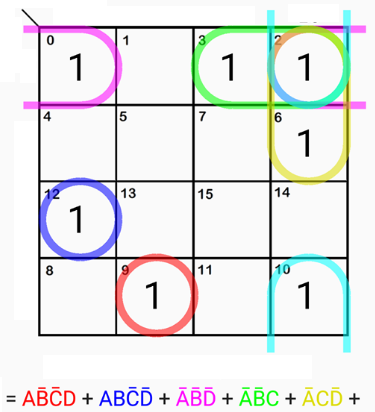
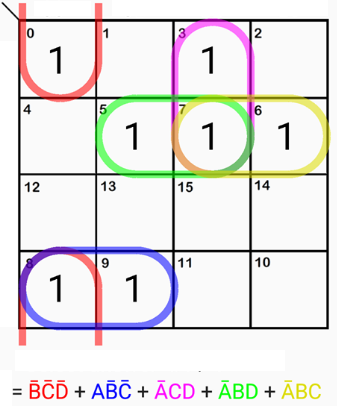
Fe (A,B,C) = (1,3,5,7,8)

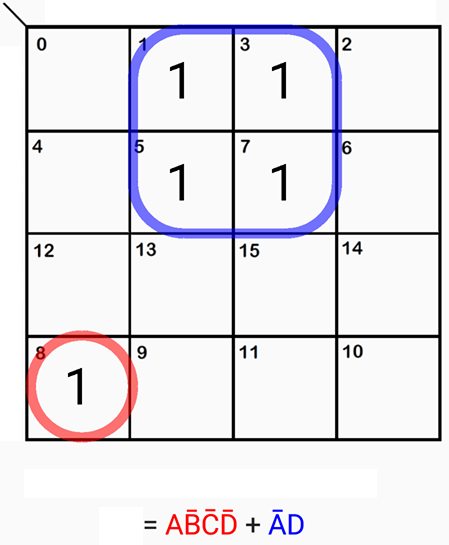
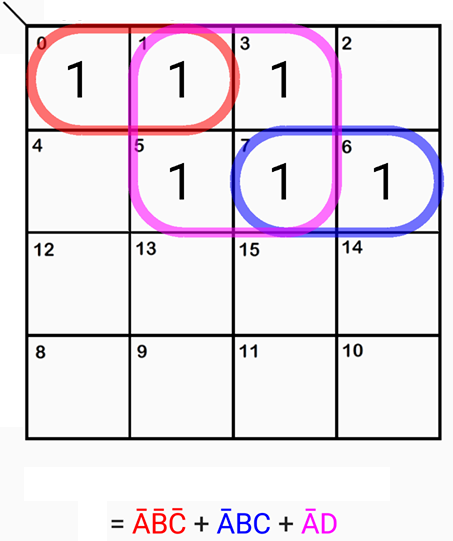
Ff (A,B,C) = (0,1,3,5,6,7)

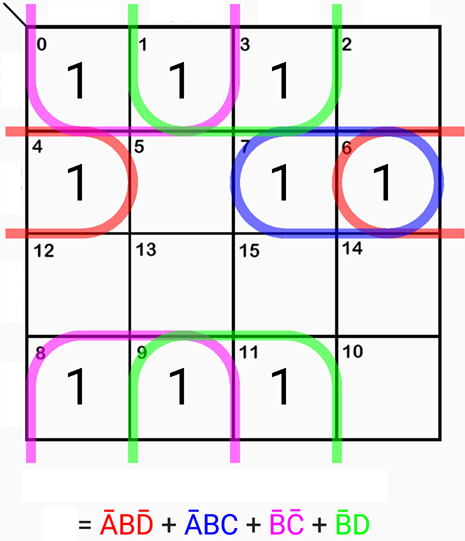
Fg (A,B,C) = (0,1,3,4,6,7,8,9,11)

**Karnaugh map (K-map):**

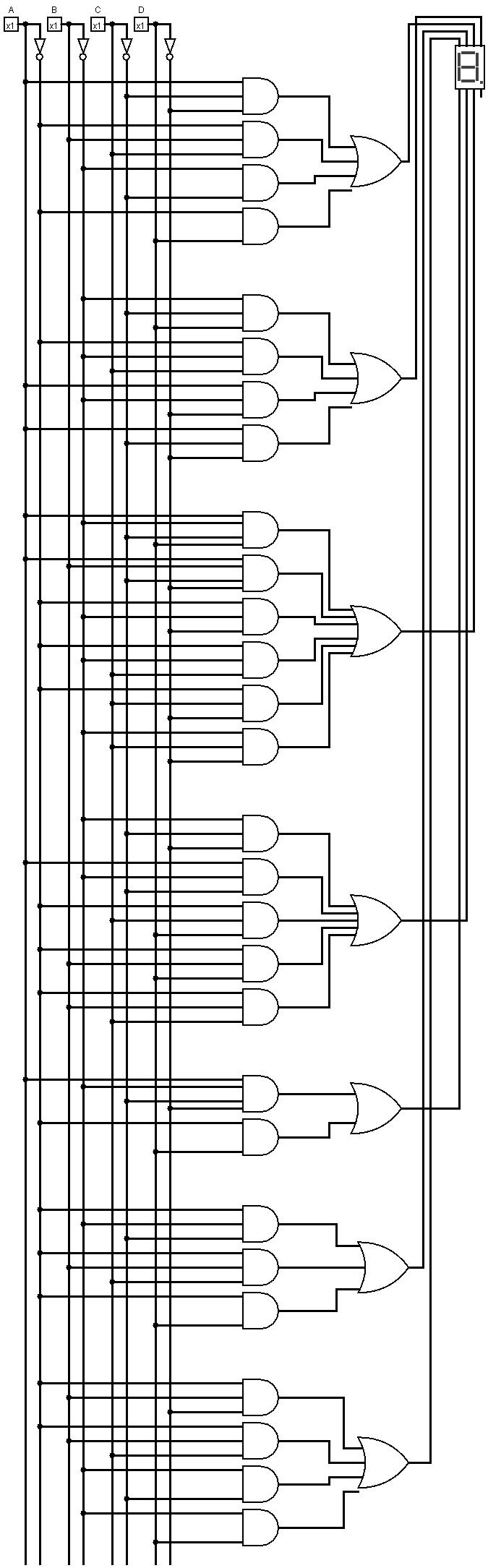
** **

** **

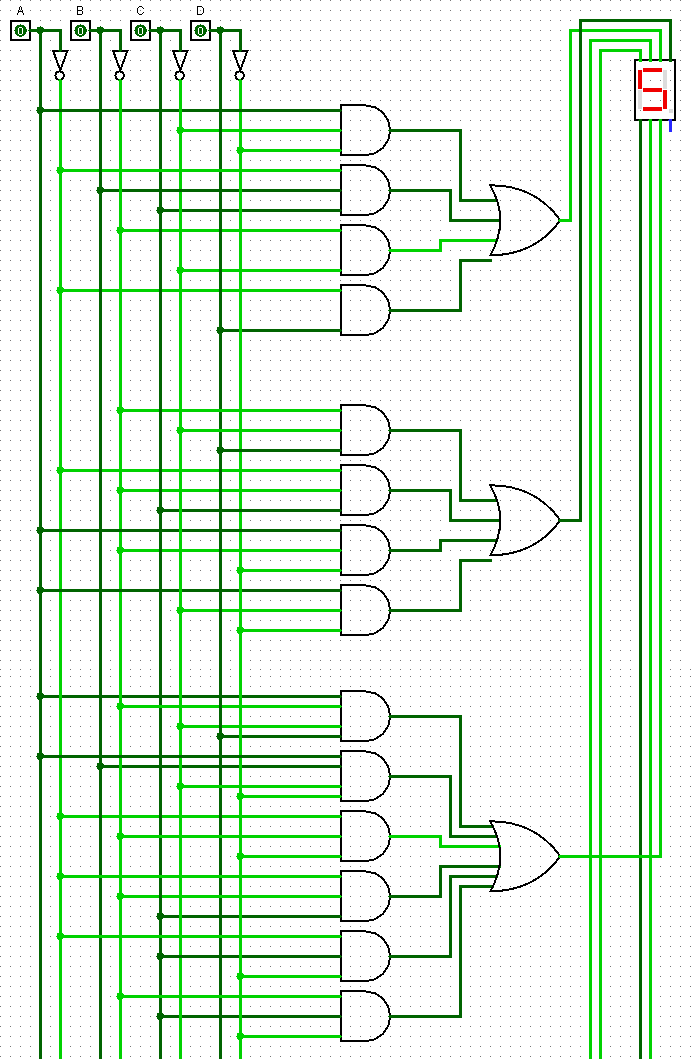
** **

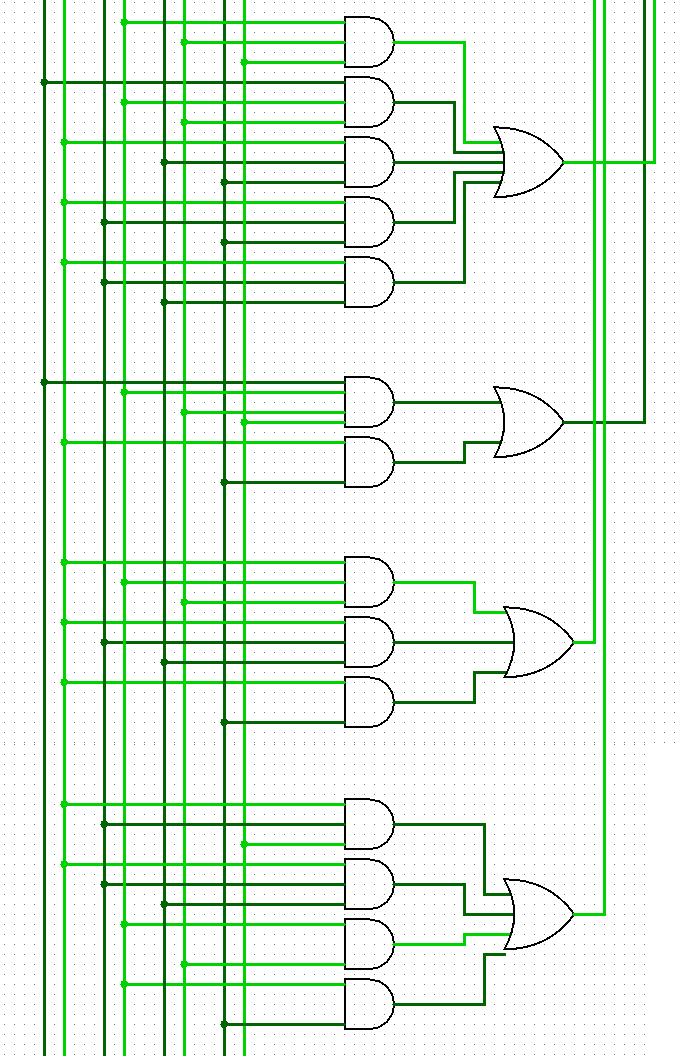
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**Circuit Diagram:**

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**Simulation:**

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**Part B (Using Decoder)**

**Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **A** | **B** | **C** | **D** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| **0** | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| **1** | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| **2** | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| **3** | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| **4** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **5** | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| **6** | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| **7** | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| **8** | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| **9** | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| **10** | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| **11** | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| **12** | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| **13** | 1 | 1 | 0 | 1 | x | x | x | x | x | x | x |
| **14** | 1 | 1 | 1 | 0 | x | x | x | x | x | x | x |
| **15** | 1 | 1 | 1 | 1 | x | x | x | x | x | x | x |

a= Y0 + Y1 + Y3+ Y5 + Y6+ Y7+ Y8 + Y9 + Y12

b= Y1 + Y2 + Y3 + Y8 + Y9 + Y10 + Y12

c= Y0 + Y2 + Y3 + Y6 + Y9 + Y10 + Y12

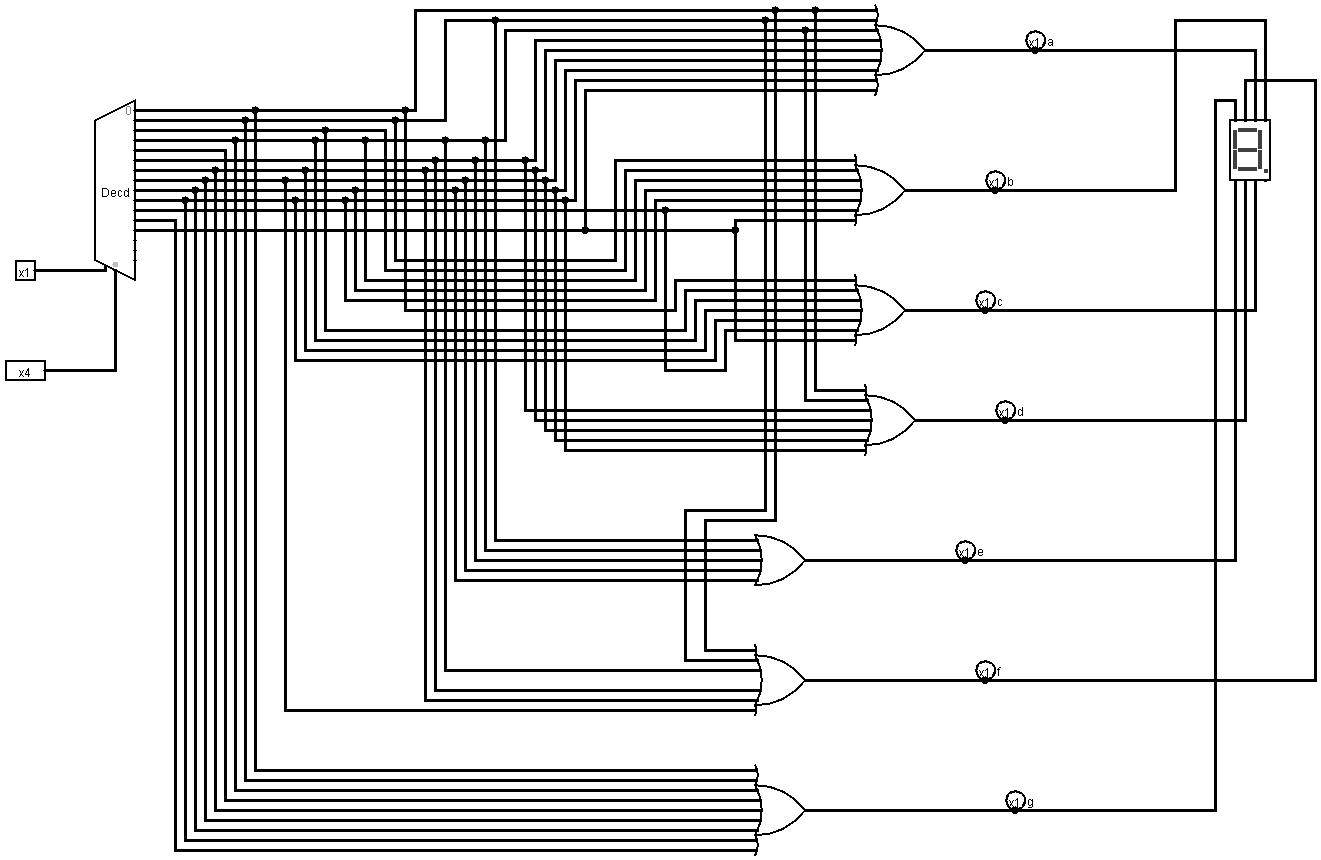
d= Y0 + Y3 + Y5 + Y6 + Y7 + Y8 + Y9

e= Y1 + Y3 + Y5 + Y7 + Y8

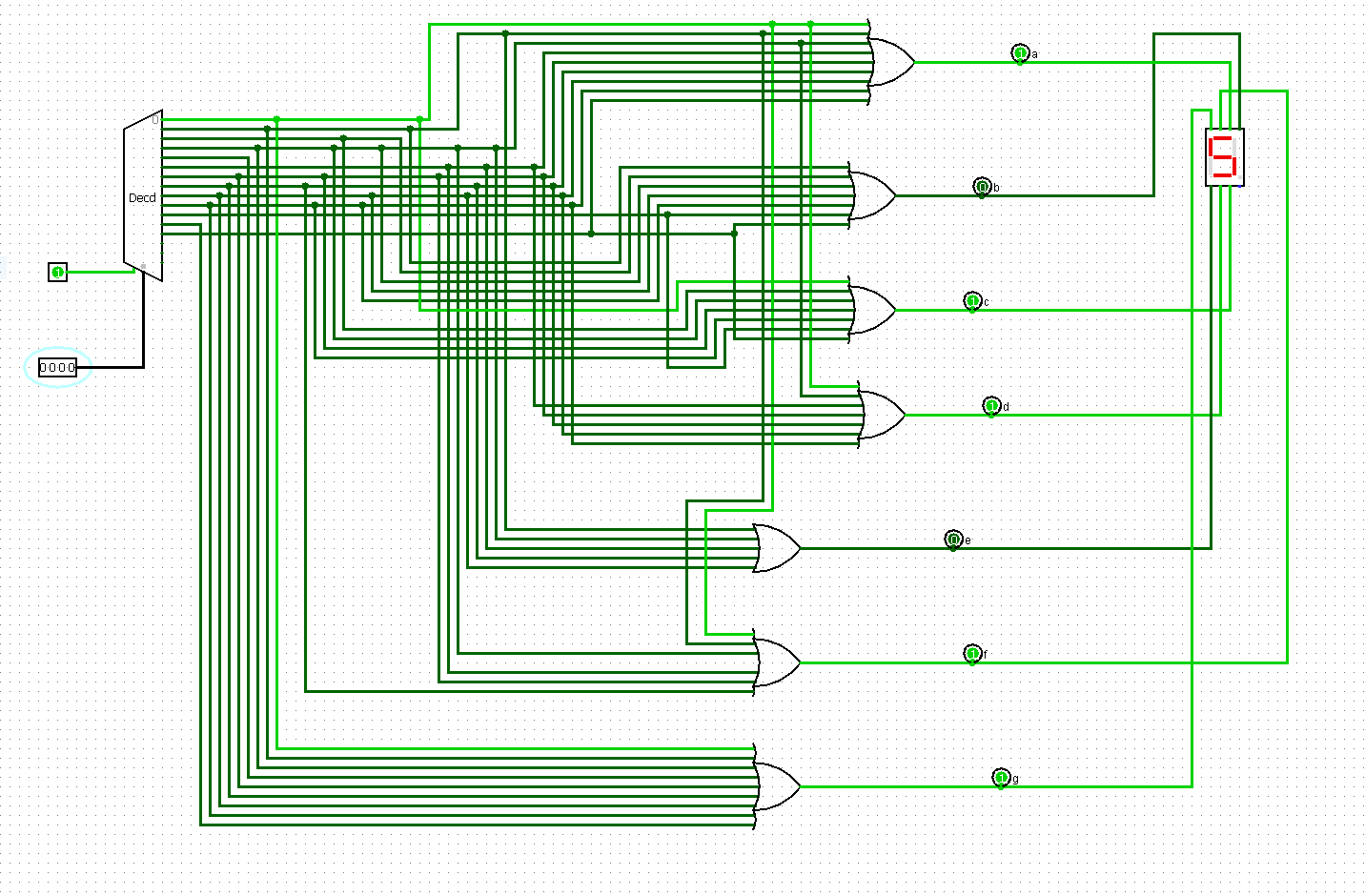
f= Y0 + Y1 + Y3 + Y5 + Y6 + Y7

g= Y0 + Y1 + Y3 + Y4 + Y6 + Y7 + Y8 + Y9 + Y11

**Circuit Diagram:**

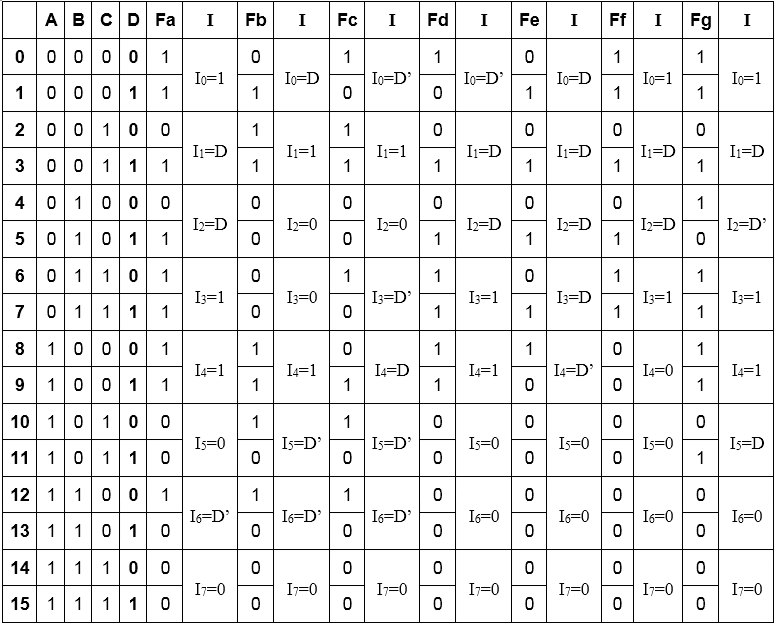
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**Simulation:**

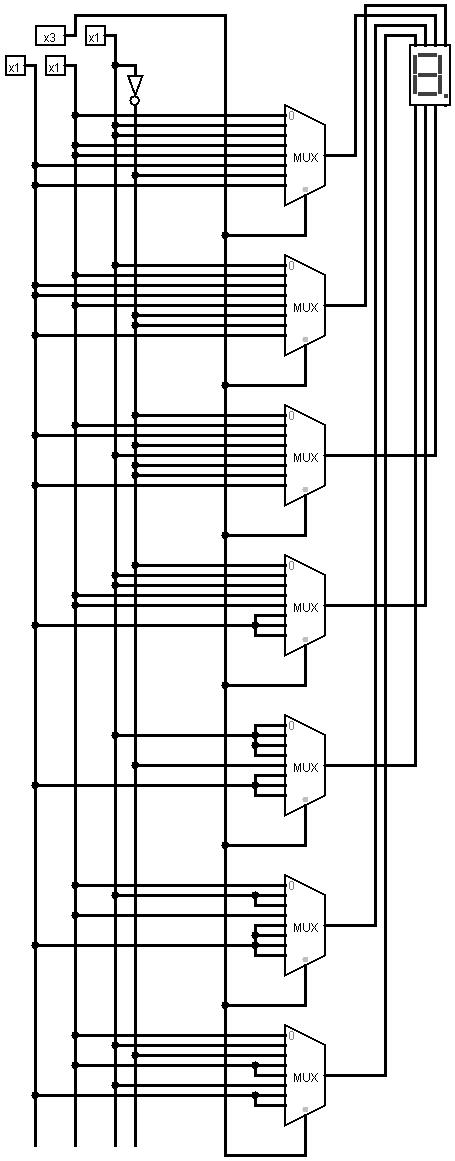
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**Part C (Using 8:1 MUX)**

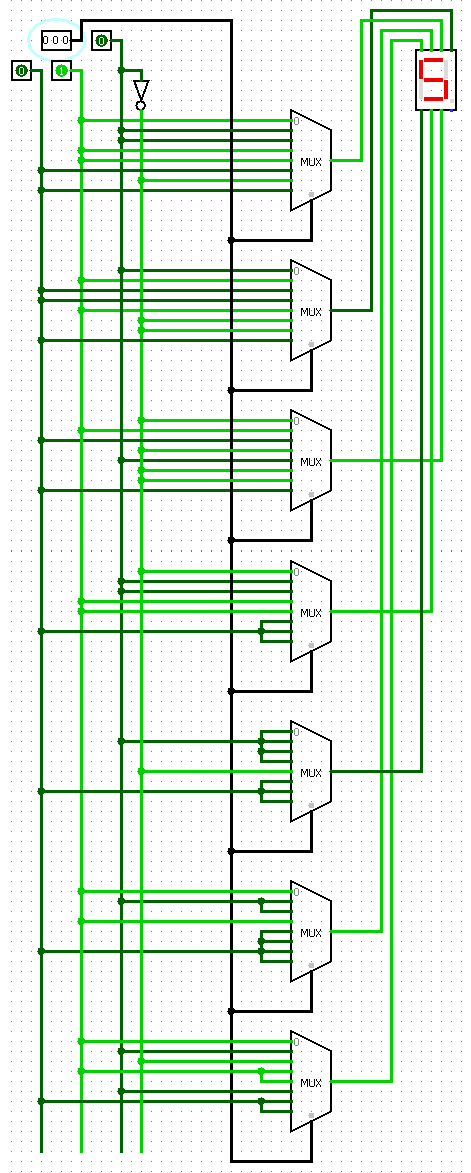
**Truth Table:**

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**Block Diagram:**

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**Simulation:**

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**Explanation**:

From the truth table it can be seen that, the number of input bits is four (A,B,C,D) and the number of output bits is seven (Fa,Fb,Fc,Fd,Fe,Ff,Fg). We have assigned the number (0-12) for the inputs. We have considered 0 (zero) for the last three inputs. Afterwards,we have constructed the truth table accordingly and with the help of the K-map we obtained minimal term for each of the seven output functions (Fa,Fb,Fc,Fd,Fe,Ff,Fg). Later, we have simulated the circuit with logisim with basic gates, 3:8 decoder and 8:1 multiplexer.

However, we have chosen to conduct the experiment using multiplexer. Behind this decision we had to consider a few facts for instance number of bits, efficiency, complexity, cost consideration etc.

From the above given figure it can be seen that for both basic gates and decoder the Literal cost (L), Gate input cost (G), Gate input cost including inverters (GN) are much higher than the multiplexer. Also it will be a very complicated circuit where relatively more wiring is required and also the cost of implementation is higher. Thus we have decided to use multiplexer to implement the circuit.